

# Modernizing Parallel Code with Pattern Analysis

## Supplementary Material: Additional Pattern Definitions

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This supplement completes the definitions provided in Section 4 of Castañeda Lozano *et al.*'s PPOPP '21 paper [1].

**Conditional maps.** Conditional maps are modeled as regular maps except that their last constraints are replaced by constraints requiring that only *some* components have outgoing arcs:

$$\begin{aligned} \exists c \in M, \exists \langle u, v \rangle \in \text{arcs}(DDG) : \\ u \in \text{nodes}(c) \wedge v \notin \text{nodes}(c) \end{aligned} \quad (1a)$$

$$\begin{aligned} \wedge \exists c \in M, \nexists \langle u, v \rangle \in \text{arcs}(DDG) : \\ u \in \text{nodes}(c) \wedge v \notin \text{nodes}(c) \end{aligned} \quad (1b)$$

**Linear map-reductions.** A *linear map-reduction* within *DDG* is a tuple  $\langle M, R \rangle$  where *M* is a map (2a), *R* is a linear reduction (2b), and both are subject to channeling constraints as specified in (2c-2d).

In a linear map-reduction, each map component produces an output data element that is only taken as input by its corresponding reduction component. This is modeled by requiring that all nodes in each map component can reach the nodes of its corresponding component in the linear reduction (2c), and forbidding all other arcs between the map and the linear reduction (2d).

$$\begin{aligned} \text{linear-map-reduction}(\langle M, R \rangle, DDG) \iff \\ \text{map}(M, DDG) \end{aligned} \quad (2a)$$

$$\wedge \text{linear-reduction}(R, DDG) \quad (2b)$$

$$\begin{aligned} \wedge \forall i \in [1, n], \forall u \in \text{nodes}(M_i), \forall v \in \text{nodes}(R_i) : \\ \text{reaches}(u, v) \end{aligned} \quad (2c)$$

$$\begin{aligned} \wedge \forall i, j \in [1, n] \mid i \neq j, \nexists \langle u, v \rangle \in \text{arcs}(DDG) : \\ u \in \text{nodes}(M_i) \wedge v \in \text{nodes}(R_j) \end{aligned} \quad (2d)$$

**Tiled map-reductions.** A *tiled map-reduction* within *DDG* is a tuple  $\langle M, \langle RP, RF \rangle \rangle$  where *M* is a map (3a),  $\langle RP, RF \rangle$  is a tiled reduction (3b), and both are subject to channeling constraints as specified in (3c-3e).

In a tiled map-reduction, each map component produces an output data element that is only taken as input by its corresponding partial reduction component. This is modeled by requiring that all nodes in each map component can reach the nodes of its corresponding partial reduction component (3c), and forbidding all other arcs between the map

and the tiled reduction (3d-3e).

$$\begin{aligned} \text{tiled-map-reduction}(\langle M, \langle RP, RF \rangle \rangle, DDG) \iff \\ \text{map}(M, DDG) \end{aligned} \quad (3a)$$

$$\wedge \text{tiled-reduction}(\langle RP, RF \rangle, DDG) \quad (3b)$$

$$\begin{aligned} \wedge \forall i \in [1, n], \forall u \in \text{nodes}(M_i), \\ \forall v \in \text{nodes}(RP_{(i \text{ div } m + 1)(i \text{ mod } m + 1)}) : \text{reaches}(u, v) \end{aligned} \quad (3c)$$

$$\begin{aligned} \wedge \forall i \in [1, n], \forall j \in [1, m], \\ \forall k \in [1, p] \mid j \neq i \text{ div } m + 1 \wedge k \neq i \text{ mod } m + 1, \\ \nexists \langle u, v \rangle \in \text{arcs}(DDG) : \\ u \in \text{nodes}(M_i) \wedge v \in \text{nodes}(RP_{jk}) \end{aligned} \quad (3d)$$

$$\begin{aligned} \wedge \forall i \in [1, n], \forall j \in [1, m], \nexists \langle u, v \rangle \in \text{arcs}(DDG) : \\ u \in \text{nodes}(M_i) \wedge v \in \text{nodes}(RF_m) \end{aligned} \quad (3e)$$

## References

- [1] Roberto Castañeda Lozano, Murray Cole, and Björn Franke. 2021. Modernizing Parallel Code with Pattern Analysis. In *Principles and Practice of Parallel Programming*. ACM.